

# RAVI KUKRETI

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## EDUCATION

### NSIT (DELHI UNIVERSITY)

M.TECH IN EMBEDDED AND VLSI  
Dwarka, New Delhi  
Cum. GPA: 7.67

### GRAPHIC ERA UNIVERSITY

B.TECH IN ECE  
Dehradun | Cum. GPA: 7.4

### ARMY SCHOOL DEHRADUN HSC

CLEMENTTOWN | PERCENTAGE: 71

### ARMY SCHOOL DEHRADUN SSC

CLEMENTTOWN | PERCENTAGE: 73.2

## COURSEWORK

### GRADUATE

Digital Integrated Circuit  
Semiconductor Devices and Memories  
Analog Integrated Circuit  
STA(udemy course)  
Processor Design  
Device Modelling and Circuit simulation

## SKILLS

### PROGRAMMING

Verilog  
SystemVerilog  
C basics  
TCL (CLI)

### TOOL

Vim  
Eldo(Mentor Graphics)  
LT-spice  
Xilinx  
Questa Sim

## ACHIEVEMENTS

IEEE Conference research paper on  
Implementation of Probability Using FIR  
filter.(2014)

IEEE research paper on Performance  
Optimization of Digital CMOS logic  
circuits using LE theory and APSO.(2019)

GATE Percentile 98.67(2016)

GATE Percentile 98.53(2018)

## EXPERIENCE

### TRUECHIP SOLUTIONS | TRAINING

Jan 2019 – Apr 2019 | Noida, UP

- Deep learning of hardware descriptive and verification language using Verilog and SystemVerilog. understanding of verification environment using UVM methodology.

## PROJECT

### DESIGN AND VERIFICATION OF 8B9B ENCODER

May 2019 – July 2019 | Noida, UP

- Encoding 8bit into 9bit and writing DUT using SystemVerilog.
- A verification environment is created using UVM methodology to verify the correct functionality of DUT.

### OPTIMUM TRANSISTOR SIZING OF CMOS LOGIC CIRCUIT USING LE THEORY AND APSO ALGORITHM

Jan 2019 – Apr 2019 | Dwarka, New Delhi

- Using LE theory transistor Delays are optimized and with the help of nature inspired algorithm i.e APSO iteration on transistor size provide minimum area and power, hence improved PDAP.

### PROGRAMMABLE CIRCUIT USING MEMRISTOR

Aug 2018 – Dec 2018 | Dwarka, New Delhi

- Memristors are used to develop oscillator circuits, RC phase shift oscillator, Comparator circuit.
- With the help of triggering pulse memristor are used as memory devices storing logical bit values.

### DESIGN AND IMPLEMENTATION OF 8BIT RISC PROCESSOR

Sep 2017 – Nov 2017 | Dwarka, New Delhi

- Implementation of various unit such as control unit, data path unit and memory unit with the help of Verilog HDL.

## RESEARCH

### VLSI DESIGN LAB | HEAD POSTGRAD RESEARCH

Jan 2019 – Apr 2019 | Dwarka, New Delhi

Worked with **Dr. Kunwar Singh**

- Automation of CMOS transistor sizing and improving PDAP.

## POSITION OF RESPONSIBILITY

### NSIT- NEW DELHI | TEACHING ASSISTANTSHIP

Aug 2017 – Apr 2019 | Dwarka, New Delhi

Teaching Assistantship in Embedded and VLSI labs.